SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD OF THE SAME

BACKGROUND

The semiconductor industry has experienced rapid growth due to continuous improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, which allows more components to be integrated into a given area. However, the smaller feature size may lead to more leakage current. As the demand for even smaller electronic devices has grown recently, there has grown a need for reducing leakage current of semiconductor devices.

In a complementary metal oxide semiconductor (CMOS) field effect transistor (FET), active regions include a drain, a source, a channel region connected between the drain and the source, and a gate on top of the channel to control the on and off state of the channel region. When the gate voltage is more than a threshold voltage, a conductive channel is established between the drain and the source. As a result, electrons or holes are allowed to move between the drain and source. On the other hand, when the gate voltage is less than the threshold voltage, ideally, the channel is cut off and there are no electrons or holes flowing between the drain and the source. However, as semiconductor devices keep shrinking, due to the short channel leakage effect, the gate cannot fully control the channel region, especially the portion of the channel region which is far away from the gate. As a consequence, after semiconductor devices are scaled into deep sub-30 nanometer dimensions, the corresponding short gate length of conventional planar transistors may lead to the inability of the gate to substantially turn off the channel region.

As semiconductor technologies evolve, fin field effect transistors (FinFETs) have emerged as an effective alternative to further reduce leakage current in semiconductor devices. In a FinFET, an active region including the drain, the channel region and the source protrudes up from the surface of the semiconductor substrate upon which the FinFET is located. The active region of the FinFET, like a fin, is rectangular in shape from a cross section view. In addition, the gate structure of the FinFET wraps the active region around three sides like an upside-down U. As a result, the gate structure's control of the channel has become stronger. The short channel leakage effect of conventional planar transistors has been reduced. As such, when the FinFET is turned off, the gate structure can better control the channel so as to reduce leakage current.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** shows a top view of a wafer having an edge portion and a center portion.

FIG. **2** shows a top view of a substrate having an edge portion and a center portion.

FIG. **3**A shows a top view of a die having a dense-patterned region and an isolated-patterned region.

FIG. **3**B shows a top view of a die having a dense-patterned region and an isolated-patterned region.

FIG. **4** shows a perspective view of a FinFET structure, in accordance with some embodiments of the present disclosure.

FIG. **5** shows a cross sectional view of a FinFET structure, in accordance with some embodiments of the present disclosure.

FIG. **6** shows a cross sectional view of an isolated-patterned FinFET structure in an edge portion and in a center portion, in accordance with some embodiments of the present disclosure.

FIG. **7** shows a cross sectional view of a dense-patterned FinFET structure in an edge portion and in a center portion, in accordance with some embodiments of the present disclosure.

FIG. **8** shows a cross sectional view of a dense-patterned FinFET structure in an edge portion and an isolated-patterned FinFET structure in a center portion, in accordance with some embodiments of the present disclosure.

FIG. **9**A shows a spectroscopic critical dimension mapping of a degree of notching, in accordance with some embodiments of the present disclosure.

FIG. **9**B shows a spectroscopic critical dimension mapping of a degree of notching, in accordance with the conventional art.

FIG. **10** to FIG. **16** show fragmental cross sectional views of a method for manufacturing a semiconductor structure on a substrate, in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

Along with the decrease of the feature dimension in a field effect transistor (FET), the topography and structural uniformity are gaining less control. For example, a bottom gate profile in a FinFET structure can be either notching or footing, depending on the patterning environment (e.g. isolated pattern or dense pattern) and the position (e.g. edge